METHOD FOR PREVENTING TO FORM A SPACER UNDERCUT IN SEG PRE-CLEAN PROCESS

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a method of preventing to form a spacer undercut, and more particularly to a method of etching the oxide and nitride spacer simultaneously to prevent from forming a spacer undercut in SEG Pre-clean process.

2. DESCRIPTION OF THE PRIOR ART

Generally, as semiconductor dimensions continue to shrink and device densities increase, contact resistance and junction depth become increasingly critical for device performance. Raised source and drain structures can provide shallow junctions with low series resistance, enhancing performance. Raised source and drain structures are typically fabricated using selective epitaxial growth (SEG) method which need a clean surface of silicon substrate; however, the surface of silicon substrate is accessible to form a native oxide with aqueous and oxygen atom from the air, for instance a silicon dioxide layer. Therefore, it is generally utilized hydrofluoric acid (HF) solution to remove the native oxide on the silicon substrate. However, employing hydrofluoric acid in order to remove the oxide on the silicon substrate that will produce a spacer

undercut and result in leakage current between source, drain and gate.

The formation of an undercut is due to the wet etching. A thin film will be generated two kinds of profile after etching process, which is isotropic and anisotropic etching profile respectively. Also, the wet etching is belonged to isotropic etching and chemical reaction that does not have any direction when performing a reaction. It will produce lateral and vertical etching simultaneously; therefore, the undercut is created.

Typically, the Pre-clean process before performing SEG in raised source and drain modules is described as in FIG. 1A and FIG. 1B. Referring to FIG 1A, a semiconductor substrate 101 is provided firstly; for instance a p-type or n-type silicon substrate. Then, a plurality of isolation is formed in the semiconductor substrate 101; for instance a plurality of isolation is formed by shallow trench isolation (STI) process. A gate oxide 105 and a gate electrode 107 are sequentially formed between the plurality of isolation. Next, a spacer 109 of the double-film structure is formed on the side-wall gate oxide 105 and side-wall gate electrode 107; wherein the spacer 109 comprises a silicon dioxide layer 109A and a silicon nitride layer 109B. Referring to FIG. 1B, an epi-layer is formed subsequently as raised source and drain 113 on the exposed semiconductor substrate 101 by selective epitaxial growth (SEG) and chemical vapor deposition (CVD) method. However, it need the clean surface of the semiconductor substrate 101 prior to forming the epi-layer by SEG technique so that a way of wet etching, which utilizes DHF (HF in deionized water), will remove the native oxide on the semiconductor substrate 101. As a result, the hydrofluoric acid; wherein the HF is diluted in deionized water (1/100 in

volume%), will also etch the silicon dioxide layer 109A of the spacer 109. Therefore, an undercut 111 will be created within the silicon dioxide spacer. Also, after raised source/drain 113 is deposited by SEG technique, the undercut 111 will generate defects between raised source/drain 113 and gate 107, further; leakage current will be produced. In addition, the epi-layer will be selectively grown under the spacer 109 and toward to gate electrode 107; therefore, it will result in bridge effect after forming salicide between raised source/drain 113 and gate 107.

Due to the fact that utilizes a hydrofluoric acid solution in order to remove the native oxide, a spacer undercut is created and result in leakage current between source, drain and gate. Therefore, the present invention provides a method for preventing to form a spacer undercut in SEG Pre-clean process.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method for providing an improved etching process which utilizes a HFEG (HF diluted by ethylene glycol) solution to etch oxide and nitride simultaneously. Compare to oxide, nitride is etched comparatively faster than oxide is. It is an objective of the present invention to provide a method for improvement in formation of an undercut in Pre-clean process that utilizes a hydrofluoric acid solution to remove the native oxide on the semiconductor substrate in the prior art. It is another objective of the present invention is that provides a method for obtaining a clean surface of the semiconductor in order to form raised source and drain structure with SEG technique. It is yet another objective of the present invention is that

provides a method for preventing leakage current is formed between raised source/drain and gate because of formation of the spacer undercut in Pre-clean process.

According to a preferred embodiment of the present invention, a semiconductor substrate is provided firstly which comprises a plurality of isolation, and then a gate structure is formed on the semiconductor substrate that comprises a gate oxide and a polysilicon gate electrode thereof. Following, a first spacer is formed on the side-wall polysilicon gate electrode and side-wall gate oxide; for instance a silicon dioxide spacer. Then, a second spacer is formed on the side-wall first spacer; for instance a silicon nitride spacer. As a result, there is a native oxide on the semiconductor substrate, and it is necessary to clean the surface of the semiconductor with DHF before forming the raised source and drain with SEG. While using DHF to clean the surface of the semiconductor, the first spacer is etched partially so that a spacer undercut is created. Subsequently, the second spacer and the first spacer are removed partially by a HFEG solution in order to obtain a negligible undercut within the first spacer, meanwhile; the native oxide on the semiconductor surface is removed. Hence, a clean surface of the semiconductor substrate is obtained. Finally, raised source and drain structure is formed on the surface of the semiconductor substrate with SEG technique.

BRIEF DESCRIPTION OF THE DRAWINGS

The objectives and features of the present inventions as well as advantages thereof will become apparent from the following detailed description,

considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings, which are not to scale, are designed for the purpose of illustration and not as a definition of the limits of the invention, for which reference should be made to the appended claims.

The present invention can be the best understood through the following description and accompanying drawings, wherein:

FIG. 1A to 1B shows schematically cross-sectional views of various steps of a conventional method for Pre-clean process; and

FIG. 2A to 2E shows schematically cross-sectional views of various steps of the present method for preventing a spacer undercut is formed in Pre-clean process according to one embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Preferred embodiment of this invention will be explained with reference to the drawings of FIG. 2A to 2E. Referring to FIG. 2A, a semiconductor substrate 201 is provided firstly; for instance silicon dioxide. An oxide layer (not illustrated) is deposited on the semiconductor substrate 201; for instance silicon dioxide. A dielectric layer (not illustrated) is deposited on the oxide layer; for instance silicon nitride. The oxide and nitride layers are defined as a mask layer of an active region in the semiconductor substrate 201. Thereafter, etching a portion of the mask layers through a dry etching process, and dry etching is performed and stopped within the semiconductor substrate 201 so as to form a plurality of shallow trench. Then, the surfaces of shallow trench

have an oxidation so that the damage on the shallow trench surface will be filled and repaired. Subsequently, performing trench filling with silicon dioxide by chemical vapor deposition (CMP) technique and planarizing the trench oxide layer by chemical mechanical polishing (CMP) technique so that a plurality of isolation 203 is formed, which can provide a isolation between each semiconductor device through subsequent processes. Following, a gate structure, which comprises a thin gate oxide 205 and a polysilicon gate electrode 207 thereof, is formed sequentially on the semiconductor substrate 201 and between a pair of isolation 203, wherein the polysilicon gate electrode 207 is formed upon the gate oxide 205.

Subsequently, referring to FIG. 2B, a pair of spacer of double-film structure 209 is formed on the side-wall of the gate structure, which comprises the polysilicon gate electrode 207 and the gate oxide 205. The spacer 209 comprises a first spacer 209A and a second spacer 209B, wherein the first spacer 209A is formed firstly on the side-wall polysilicon gate electrode 207 and the side-wall gate oxide 205, and then the second spacer 209B is formed on the side-wall first spacer 209A. More, the first spacer 209A comprises a silicon dioxide layer, and the second spacer 209B comprises a silicon nitride layer. The spacer 209 is formed by way of the following steps: At first, a conformal silicon dioxide layer 209A is formed on the semiconductor substrate 201 surface and polysilicon gate electrode 207, then, forming a silicon nitride 209B on the conformal silicon dioxide layer 209A. After that, anisotropic etching this conformal silicon dioxide layer 209A and silicon nitride layer 209B with a way of dry etching; for instance reaction ion etch (RIE) method, so the spacer 209 of double-film structure is formed. The conformal silicon dioxide

layer 209A is deposited with a way of CVD; for instance Plasma Enhanced CVD (PECVD); in addition, the silicon nitride layer 209B is deposited with a way of CVD; for instance Low Pressure CVD (LPCVD) or tetraethylorthosilicate CVD (TEOS-CVD). As a result, a native oxide 202 is accessible to form by oxide and aqueous atom from the air; for instance silicon dioxide. Also, raised source and drain is formed by SEG technique; however, the epitaxial is only selectively growth on the silicon substrate surface with SEG technique, whereas oxide and nitride will not. Therefore, it is necessary to have a clean surface of semiconductor substrate 201 that performs a Pre-clean process to remove the native oxide 202 prior to forming raised source and drain.

Referring to FIG. 2C, utilizing a hydrofluoric acid solution to remove a portion of native oxide 202 so that a remaining native oxide 202B is formed on the semiconductor substrate 201. The hydrofluoric acid is diluted in deionized water (DHF), wherein the volume ratio for deionized water to hydrofluoric acid is about 10:1-100 : 1, the preferred ratio is about 100:1. When removing the native oxide 202 by HF, it will produce an undercut with a sunken profile due to the fact that the wet etching is belonged to isotropic etching. Therefore, the first spacer 209A of silicon dioxide layer and the native oxide 202 will be partially etched, more, when horizontal etching is performed to etch first spacer 209A, a film is under the first spacer 209A will also be etched. Hence, it will produce a spacer undercut with a sunken profile within the first spacer 209A of silicon dioxide layer. The problem with a spacer undercut will generate defects between source/drain and gate after forming raised source and drain by SEG technique, further, result in leakage current thereof. Also, epitaxial is selectively growth under the spacer 207, even toward to the polysilicon gate

electrode 207. Hence, it will produce bridge effect between raised source/drain and polysilicon gate electrode 207 after forming salicide.

Accordingly, in order to solve a spacer undercut, which is an oxide film of the first spacer, is created in Pre-clean process because using hydrofluoric acid to remove a native oxide on the surface of the semiconductor substrate 201 before performing SEG technique. The present invention provides a method for improving the Pre-clean process, wherein HFEG (HF diluted by ethylene glycol) is utilized to etch the first spacer 209A of silicon dioxide and the second spacer 209B of silicon nitride simultaneously. Therefore, the undercut 211 within the first spacer 209A is removed or neglected. The HFEG solution in which the hydrofluoric acid is diluted in glycol(0-4% in volume%), and the etching selectivity is about 2 : 1 for nitride to oxide; for this reason, the etching rate of nitride is faster than oxide. Referring to FIG. 2D, etching the first spacer 209A and second spacer 209B simultaneously by HFEG. Also, the most of the second spacer 209B and a portion of the first spacer 209A are removed because the etching rate of the second spacer 209B is faster than first spacer 209A is. More, the formation of an undercut 211 is modified in the meanwhile using DHF to remove the native oxide 202, further, it can also clean the remaining oxide layer 202B on the semiconductor substrate 201. By this way, it not only removes the native oxide 202 on the surface of semiconductor substrate 201 but also obtains a clean semiconductor substrate surface. Besides, it can reduce the problems that comprise the formation of an undercut 211 within the first spacer 209A and the leakage current are produced between source/drain and gate. Finally, the Pre-clean process is successively completed.

As soon as obtain a clean semiconductor substrate 201 surface, as shown in FIG. 2E. By a selective epitaxial growth and chemical vapor deposition technique; for instance ultra-high vacuum chemical vapor deposition (UHCVD), wherein an epitaxial layer is formed as raised source and drain 213 on the exposed semiconductor substrate 201 and between plurality of isolations 203 and spacer 209. As the above-mention, the low pressure CVD method comprises dichlorosiliane (SiH_2Cl_2) as a reaction gas and the UHCVD method therein comprises disilane (SiH_4) as a reaction gas. Then, implanting dopant into raised source/drain 213 by ion implantation.

In accordance with the present invention, one of the advantages is that provides a Pre-clean process, which comprises a suitable etching solution in etching rate and etching selectivity, this is, etching the first spacer and second spacer at the same time. Hence, it can modify the first spacer undercut because of etching process by DHF to remove the native oxide on the semiconductor substrate surface. In addition, it also can prevent from producing leakage current between source/drain and gate, which is sequentially formed by a SEG method.

The preferred embodiments are only used to illustrate the present invention, not intended to limit the scope thereof. Many modifications of the preferred embodiments can be made without departing from the spirit of the present invention.